# WEST Search History

DATE: Friday, June 06, 2003

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L7 | ((monitor$3 or test$3 or measur$6) with (contact adj resistance)) and (word adj line) | 40 | L7 |
| L6 | L5 and (implant$8 or diffus$4 or buried) | 43 | L6 |
| L5 | L4 and word | 118 | L5 |
| L4 | L3 and (measur$6 or test$3) with (contact or resistance or current or voltage) | 528 | L4 |
| L3 | ((257/48 )!.CCLS. ) | 964 | L3 |
| L2 | (word adj line) and (source adj line) and (measur$6 with (resistance or current or voltage)) | 488 | L2 |
| L1 | (word adj line) and (measur$6 with resistance) and buried and (test adj (wafer or substrate)) | 3 | L1 |

END OF SEARCH HISTORY

WEST

Generate Collection

L7: Entry 40 of 40 File: DWPI Jul 11, 2001

DERWENT-ACC-NO: 2002-326429
DERWENT-WEEK: 200236


TITLE: Method for manufacturing semiconductor memory device with contact resistance measurement pattern

INVENTOR: CHO, N H; MUN, W

PATENT-ASSIGNEE:

| ASSIGNEE | CODE |
|---|---|
| HYNIX SEMICONDUCTOR INC | HYNIN |

PRIORITY-DATA: 1999KR-0065616 (December 30, 1999)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|---|---|
| KR 2001065696 A | July 11, 2001 | | 001 | H01L027/10 |

APPLICATION-DATA:

| PUB-NO | APPL-DATE | APPL-NO | DESCRIPTOR |
|---|---|---|---|
| KR2001065696A | December 30, 1999 | 1999KR-0065616 | |

INT-CL (IPC): H01 L 27/10

ABSTRACTED-PUB-NO: KR2001065696A

BASIC-ABSTRACT:

NOVELTY - A method for manufacturing a semiconductor memory device with a contact resistance measurement pattern is provided to measure easily a contact resistance between a cell active region and a plug by forming a contact resistance measurement pattern.

DETAILED DESCRIPTION - A word line is formed on a cell region of a semiconductor substrate(2). A source/drain(8a) is formed on the cell region. The first dopant region(8b) is formed on a pattern region of the semiconductor substrate. The second dopant region(12) is formed on the pattern region. A spacer(15) is formed at a sidewall of the word line. The first dopant region(8b) of the pattern region is exposed. A plug(16a) connected with the source/drain(8a) and the first pattern(16b) connected with the first dopant region(8b) are formed. The first interlayer dielectric(18) is formed on the whole structure. A bit line(20a) and the second pattern(20b) are formed thereon. The second interlayer dielectric(22) is formed on the whole structure. A storage node(24) is formed on the second interlayer dielectric(22) of the cell region. The third interlayer dielectric(26) is formed on the whole structure. A wiring layer(28a) is formed on the third interlayer dielectric(26) of the cell region. The first and the second electrodes(28b,28c) are formed on the third interlayer dielectric(26) of the pattern region.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: METHOD MANUFACTURE SEMICONDUCTOR MEMORY DEVICE CONTACT RESISTANCE MEASURE PATTERN

DERWENT-CLASS: U11 U14

EPI-CODES: U11-C18B5; U14-A03B7;